TD8

TD 8 / CONVERTIR UN SIGNAL ANALOG. EN DONNÉES NUM.

Objectifs pédagogiques

A la fin de cette thématique, les étudiant·e·s seront capables de :

- énumérer les caractéristiques d'un Convertisseur Analogique-Numérique (CAN) et d'un Convertisseur Numerique-Analogique (CNA).
- analyser la structure d'un CNA
- évaluer les performances d'un CAN/CNA

Activités pédagogiques

- Lectures (hors temps présentiel - en ligne)
  - ▷ Cours : Codage des informations (J. VILLEMEJANE - 2013)
  - ▷ Cours : Le Numérique et le binaire (H. BENISTY - 2016)
  - ▷ Cours : La Conversion CAN et CNA (H. BENISTY - 2014)
- Séance de **TD8**
- Séances de **TP3** et **TP4** (module TP CéTI)

Ressources Complémentaires

- Introduction aux systèmes numériques - Julien Villemejane (2016)
- Monde numérique - Julien Villemejane (2013)
- Exercices supplémentaires proposés sur eCampus (avec correction)

TD8

TD 8 / CONVERTIR UN SIGNAL ANALOG. EN DONNÉES NUM.

Exercice 1 - Conversion de signaux courants

Notions abordées

▷ rappel des fréquences mises en jeu dans les signaux habituels

Signal audio

1. Rappeler l'intervalle de fréquences des signaux audibles par l'être humain.
2. Quelle est la fréquence minimale pour échantillonner correctement un signal audio ?

   Les signaux audio « classiques » (CD audio par exemple) sont échantillonnés à une fréquence $F_{Eclassique} = 44.1\,\text{kHz}$ et chaque échantillon est codé sur 16 bits.

   Les signaux HRA (Audio Haute Résolution) sont échantillonnés à une fréquence $F_{EHRA1} = 96\,\text{kHz}$ ou $F_{EHRA2} = 192\,\text{kHz}$ et chaque échantillon est codé sur 24 bits.
3. Ces fréquences sont-elles bien choisies ?
4. Combien de niveau logique différent y a-t-il pour chacune de ces normes ?
5. Quelle quantité d'espace numérique (en octets) faut-il prévoir pour stocker une heure de données sonores :
   (a) au format « classique », stéréo ?
   (b) au format HRA-192, en 5.1 ?

Signal vidéo

On s'intéresse au capteur **CMV50000** de la société *CMOSIS*, capteur 8K@30fps - au prix d'environ 3500$ (juin 2018) dont la documentation est donnée en annexe.

1. Quelle est la taille de l'image de ce capteur ? Combien cela fait-il de pixels ?
2. Combien de convertisseurs analogique-numérique embarquent ce capteur ? Quelle est la résolution des ADC ?
3. La vitesse de transfert donnée est-elle suffisante pour prendre des images en 8K (7680 x 4320 pixels) à 30 images/seconde ?

Exercice 2 - Système numérique

Notions abordées

▷ étude d'un signal échantillonné

▷ critère de Shannon-Nyquist

Que peut-on dire des signaux suivants ?

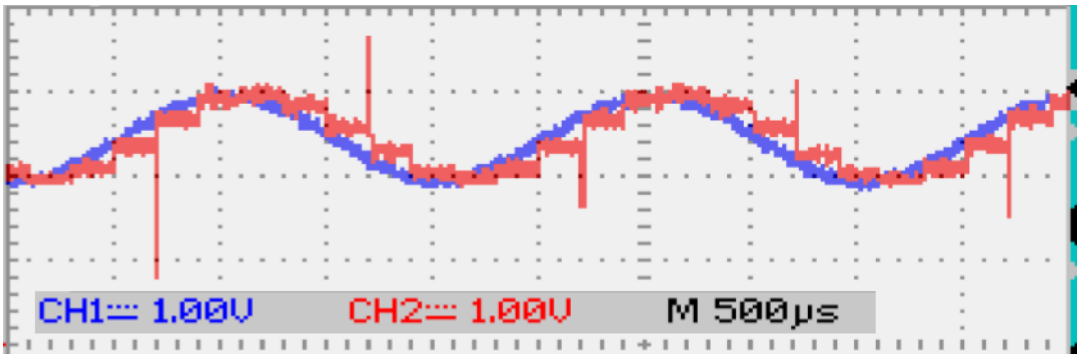


Fig. 1: Sortie d'un filtre numérique

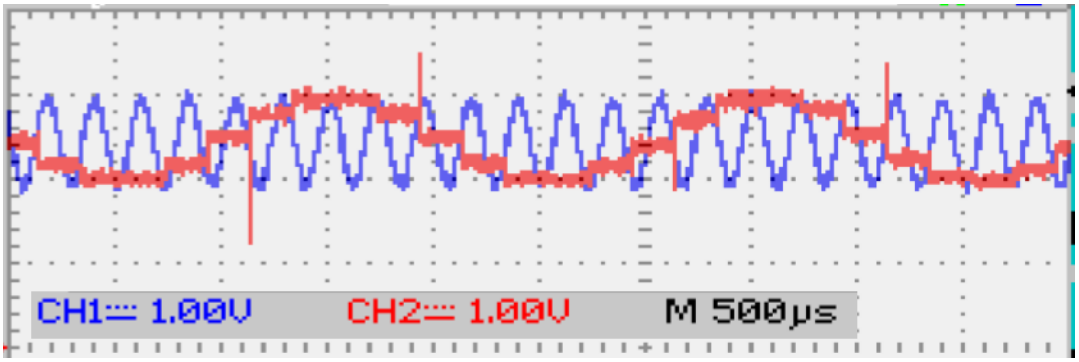


Fig. 2: Sortie d'un filtre numérique

Exercice 3 - Entrées/Sorties Numériques

Notions abordées

▷ étude de la documentation technique d'un CAN

▷ entrée/sortie série/parallèle

On s'intéresse à présent à 2 convertisseurs analogiques-numériques différents, dont une partie des documentations techniques sont données en annexe :

— **TLC548** de *Texas Instruments* (environ 3$ - juin 2018)

— **AD9230** de *Analog Devices* (environ 80$ - juin 2018)

1. A partir de ces deux documentations, remplir le tableau suivant :

	TLC548	AD9230
Type de sortie		
F_{Emax}		
Résolution		
Alimentation		

2. A l'aide de la documentation technique du **TLC548**,
   (a) Expliquer à quoi correspondent les différents éléments du **diagramme fonctionnel** donnée en page 2.
   (b) Expliquer l'opération de conversion et de récupération des données à partir de la **séquence** donnée en page 3.
   (c) Combien de temps faut-il entre chaque conversion (pour $F_{CLOCK} = 2.048\,\text{MHz}$?

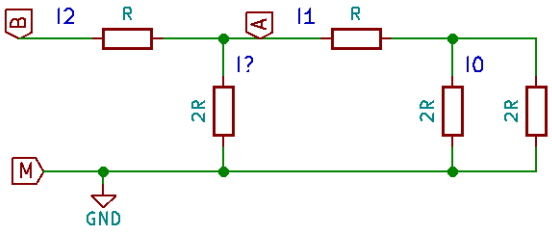
Exercice 4 - Convertisseur R-2R

Notions abordées

▷ étude de la structure d'un CNA

Montage R-2R

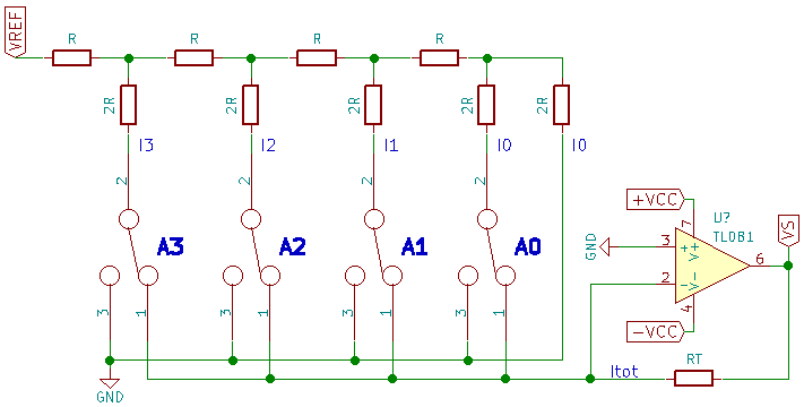
On s'intéresse à ce montage :



1. Que vaut le courant I_1 en fonction du courant I_0 (courant passant par la résistance $2R$?
2. Que vaut le courant I_2 en fonction du courant I_0 (courant passant par la résistance $2R$?

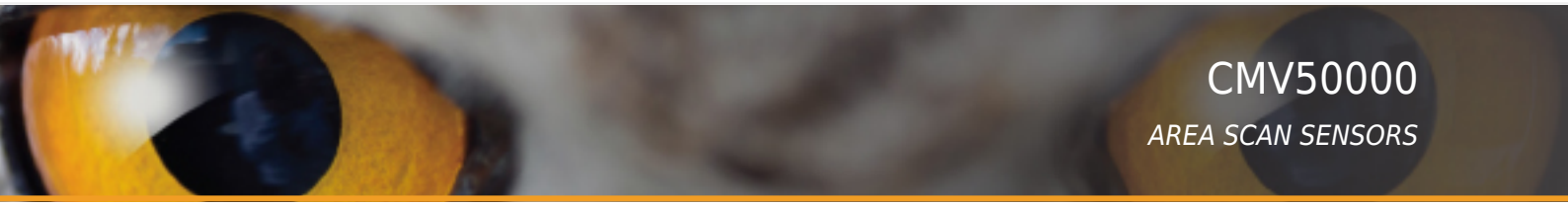
Montage complet

On s'intéresse à présent au montage suivant :



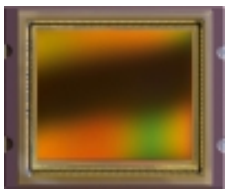
On supposera que lorsque $A_i = 0$, l'interrupteur i est en position 3 et que lorsque $A_i = 1$, l'interrupteur i est en position 1.

1. Quel est le type de montage autour de l'ALI ?
2. En quoi la structure vue précédemment peut nous aider ?
3. Que vaut alors le courant I_{tot} dans la contre-réaction de l'ALI en fonction des courants I_i ?
4. Que vaut alors le courant I_{tot} dans la contre-réaction de l'ALI en fonction du courant $I0i$ et des valeurs des A_i ?



CMV50000

AREA SCAN SENSORS



The CMV50000 is a high speed CMOS image sensor with 7920 x 6004 effective pixels (47.5Mp) developed for machine vision and video applications. The image array consists of 4.6µm pipelined 8T global shutter pixels which allow exposure during read out, while performing true CDS (Correlated Double Sampling) operation. The image sensor has 22 12bit sub-LVDS data outputs. The image sensor also integrates a programmable analog gain amplifier and offset regulation. Each output channel runs up to 830 Mbps maximum which results in 30 fps frame rate at full resolution in 12 bit. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by a dual exposure HDR mode.

SPECIFICATIONS

Part status	Sampling
Resolution	48MP - 7920 (H) x 6004 (V)
Pixel size	4.6 x 4.6
Optical format	35 mm (36.43 x 27.62 mm2)
Shutter type	Global shutter
Frame rate	30 fps
Output interface	22 LVDS @ 830 Mbps
Sensitivity	3.5 x10e7 DN/(W.s/m2) (@ 550 nm)
Conversion gain	0.272 DN/e
Full well charge	14500 e- (with binning 58000 e-)
Dark noise	8.8 e-
Dynamic range	64dB (binning: 68dB)
SNR max	41.6dB (binning: 47.6dB)
Parasitic light sensitivity	1/18000
Extended dynamic range	Yes, odd/even read out
Dark current	0.24e/s @ 20°C; 66.2e/s @60°C
Fixed pattern noise	6.6 DN rms
Chroma	Mono and RGB
Supply voltage	3.3/2.7/1.8/1.2V
Power	3W
Operating temperature range	-30°C to 70°C
RoHS compliance	Yes (TBC)
Package	141 pins PGA ceramic package
Socket	Andon Electronics (http://www.andonelectronics.com) 575-20-19A-141-01M-R27-L14 (thru-hole) 575-20-19A-141-93M-R27-L14 (surface mount)

12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter

AD9230

FEATURES

SNR = 64.9 dBFS @ f_{IN} up to 70 MHz @ 250 MSPS
ENOB of 10.4 @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
SFDR = −79 dBc @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
Excellent linearity
DNL = ±0.3 LSB typical
INL = ±0.5 LSB typical
LVDS at 250 MSPS (ANSI-644 levels)
700 MHz full power analog bandwidth
On-chip reference, no external decoupling required
Integrated input buffer and track-and-hold
Low power dissipation
434 mW @ 250 MSPS—LVDS SDR mode
400 mW @ 250 MSPS—LVDS DDR mode
Programmable input voltage range
1.0 V to 1.5 V, 1.25 V nominal
1.8 V analog and digital supply operation
Selectable output data format (offset binary, twos complement, Gray code)
Clock duty cycle stabilizer
Integrated data capture clock

APPLICATIONS

Wireless and wired broadband communications
Cable reverse path
Communications test equipment
Radar and satellite subsystems
Power amplifier linearization

FUNCTIONAL BLOCK DIAGRAM

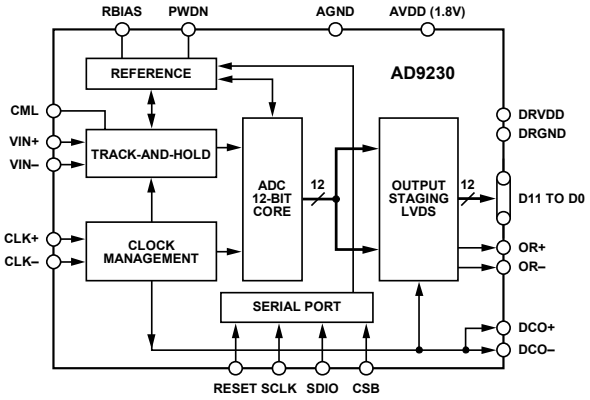


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD9230 is a 12-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates at up to a 250 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and voltage reference, are included on the chip to provide a complete signal conversion solution.

The ADC requires a 1.8 V analog voltage supply and a differential clock for full performance operation. The digital outputs are LVDS (ANSI-644) compatible and support either twos complement, offset binary format, or Gray code. A data clock output is available for proper output data timing.

Fabricated on an advanced CMOS process, the AD9230 is available in a 56-lead LFCSP, specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High Performance—Maintains 64.9 dBFS SNR @ 250 MSPS with a 70 MHz input.
2. Low Power—Consumes only 434 mW @ 250 MSPS.
3. Ease of Use—LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample and hold provide flexibility in system design. Use of a single 1.8 V supply simplifies system power supply design.
4. Serial Port Control—Standard serial port interface supports various product functions, such as data formatting, disabling the clock duty cycle stabilizer, power-down, gain adjust, and output test pattern generation.
5. Pin-Compatible Family—10-bit pin-compatible family offered as AD9211.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

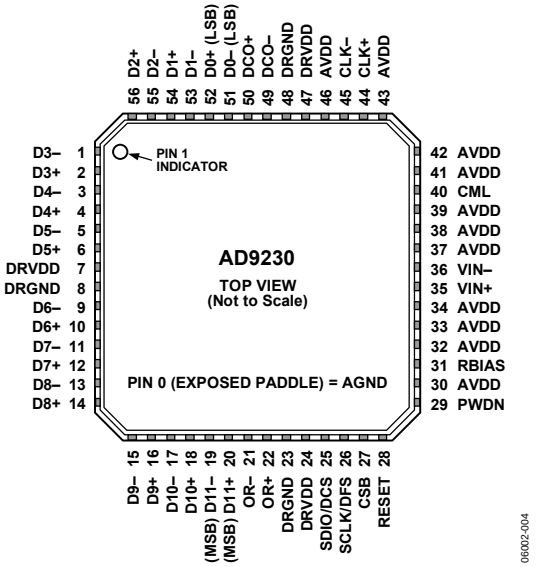


Figure 4. Single Data Rate Mode

Table 7. Single Data Rate Mode Pin Function Descriptions

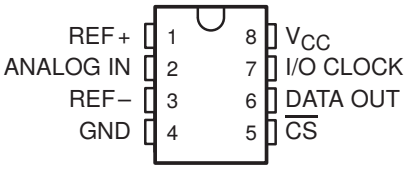
Pin No.	Mnemonic	Description
30, 32 to 34, 37 to 39, 41 to 43, 46	AVDD	1.8 V Analog Supply.
7, 24, 47	DRVDD	1.8 V Digital Output Supply.
0	AGND[1]	Analog Ground.
8, 23, 48	DRGND[1]	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Common-Mode Output Pin. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN–.
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% 10 kΩ resistor terminated to ground.) Nominally 0.5 V.
28	RESET	CMOS-Compatible Chip Reset (Active Low).
25	SDIO/DCS	Serial Port Interface (SPI®) Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
29	PWDN	Chip Power-Down.
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
51	D0–	D0 Complement Output Bit (LSB).
52	D0+	D0 True Output Bit (LSB).
53	D1–	D1 Complement Output Bit.
54	D1+	D1 True Output Bit.
55	D2–	D2 Complement Output Bit.
56	D2+	D2 True Output Bit.
1	D3–	D3 Complement Output Bit.
2	D3+	D3 True Output Bit.
3	D4–	D4 Complement Output Bit.
4	D4+	D4 True Output Bit.

TLC548C, TLC548I, TLC549C, TLC549I
8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS067C – NOVEMBER 1983 – REVISED SEPTEMBER 1996

- **Microprocessor Peripheral or Standalone Operation**
- **8-Bit Resolution A/D Converter**
- **Differential Reference Input Voltages**
- **Conversion Time . . . 17 μs Max**
- **Total Access and Conversion Cycles Per Second**
  - **– TLC548 . . . up to 45 500**
  - **– TLC549 . . . up to 40 000**
- **On-Chip Software-Controllable Sample-and-Hold Function**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **4-MHz Typical Internal System Clock**
- **Wide Supply Range . . . 3 V to 6 V**
- **Low Power Consumption . . . 15 mW Max**
- **Ideal for Cost-Effective, High-Performance Applications including Battery-Operated Portable Instrumentation**
- **Pinout and Control Signals Compatible With the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter**
- **CMOS Technology**

D OR P PACKAGE
(TOP VIEW)



description

The TLC548 and TLC549 are CMOS analog-to-digital converter (ADC) integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. These devices are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the input/output clock (I/O CLOCK) input along with the chip select ($\overline{CS}$) input for data control. The maximum I/O CLOCK input frequency of the TLC548 is 2.048 MHz, and the I/O CLOCK input frequency of the TLC549 is specified up to 1.1 MHz.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TLC548CD TLC549CD	TLC548CP TLC549CP
–40°C to 85°C	TLC548ID TLC549ID	TLC548IP TLC549IP

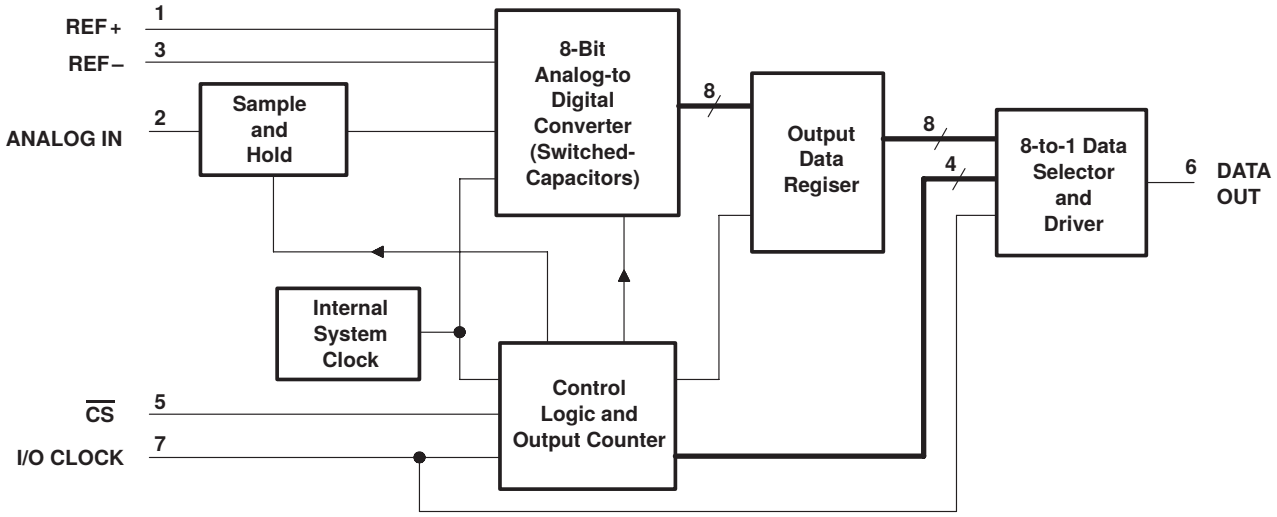
description (continued)

Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 MHz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O CLOCK together with the internal system clock allow high-speed data transfer and conversion rates of 45 500 conversions per second for the TLC548, and 40 000 conversions per second for the TLC549.

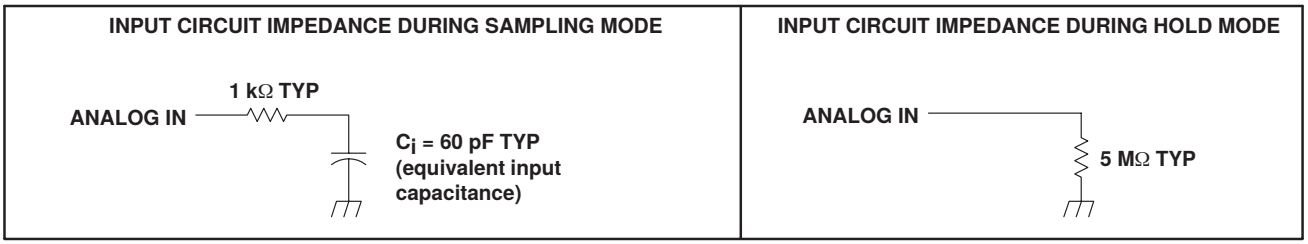
Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of ±0.5 least significant bit (LSB) in less than 17 μs.

The TLC548C and TLC549C are characterized for operation from 0°C to 70°C. The TLC548I and TLC549I are characterized for operation from –40°C to 85°C.

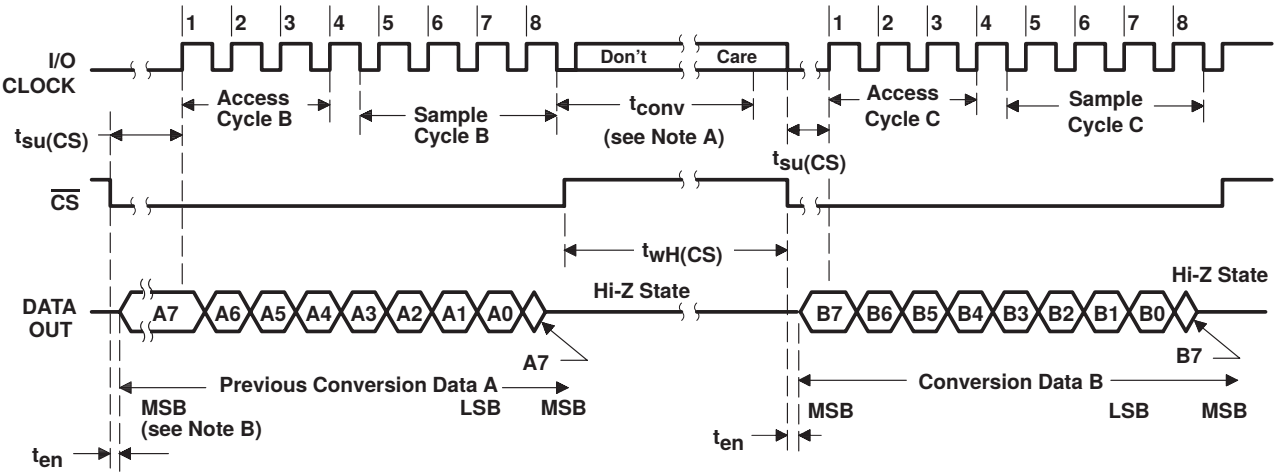
functional block diagram



typical equivalent inputs



operating sequence



NOTES: A. The conversion cycle, which requires 36 internal system clock periods (17 μs maximum), is initiated with the eighth I/O clock pulse trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.

B. The most significant bit (A7) is automatically placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) are clocked out on the first seven I/O clock falling edges. B7–B0 follows in the same manner.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range at any input	–0.3 V to V_{CC} + 0.3 V
Output voltage range	–0.3 V to V_{CC} + 0.3 V
Peak input current range (any input)	±10 mA
Peak total input current range (all inputs)	±30 mA
Operating free-air temperature range, T_A (see Note 2): TLC548C, TLC549C	0°C to 70°C
TLC548I, TLC549I	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to the network ground terminal with the REF– and GND terminals connected together, unless otherwise noted.

2. The D package is not recommended below –40°C.